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| EXAMINER | |
|---|---|
| PETRANEK, JACOB ANDREW | |
| ART UNIT | PAPER NUMBER |
| 2183 | |

| NOTIFICATION DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/059,427 | LEIJTEN, JEROEN ANTON JOHAN | |
| | Examiner | Art Unit | |
| | Jacob Petranek | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12/8/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,5-8 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

***Detailed Action***

1. Claims 1, 3, 5-8, and 16-20 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 12/8/2009

***Withdrawn Objections and Rejections***

3. The claim objections have been withdrawn due to amendment.

4. The 35 U.S.C. §112, second paragraph rejections for claims 1, 4-8, and 16-19 have been withdrawn due to amendment.

***Maintained Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 3 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites "wherein the information contains a prefetch bit whose value signals explicitly whether or not the subsequent memory line is to be prefetched." Prefetching can be defined as loading data or instructions in anticipation of their need. However, the limitations do not actually fetch instructions in anticipation of their need, they are only fetching instructions when they are needed (i.e. when an instruction has information stating that the subsequent memory line is needed.). Therefore, what is

claimed isn't prefetching as understood to one of ordinary skill in the art and is simply fetching data when it's needed. The only way that the claimed invention could possibly be considered prefetching is if the applicant is claiming a multi-cycle processor, where in the decode stage the next instruction line is fetched in anticipation of being needed a number of clock cycles in the future while the current instruction finishes executing. Since a multi-cycle processor isn't claimed, for examination purposes, the limitation prefetching will be interpreted as simply fetching a subsequent memory line in response to the information.

***Maintained Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3-4, 6-8, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. 5,819,058).

9. As per claim 1:

Miller disclosed a computer system with a processing unit and a memory, the processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines (Miller: Figure 5 elements 26, 30-36, and 172, column 8 lines 11-29 and lines 41-62), each memory line being fetched as a whole and being capable of holding more than one instruction (Miller: Figures 7 and 8, column 8

lines 11-29 and column 11 lines 58-61)(The first line in figure 7 shows VLIW packets IP0, IP1, IP2, and IP3, which results in a single memory line containing more than a single instruction. Column 8 states that 128 bits can be fetched at once, which is a memory line. Figure 8 shows an example of an entire memory line being fetched.), at least one instruction from the memory lines comprising information, inserted at compile time (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(Figure 3b is a compressed 32-bit instruction. The compiler performs the compression of the VLIW packets and inserts element 117 into the instructions to tell if the current instruction is at the end of a memory line or not. Element 117 reads upon information.), that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line (Miller: Figures 3b, 7, and 8 element 117, column 6 lines 31-35 and column 11 lines 58-67 continued to column 12 lines 1-25)(Column 6 describes a 32-bit compressed instruction containing 117 that tells if the current instruction is the last instruction within the VLIW packet. Figures 7 and 8 show examples of fetching VLIW packets from memory. IP3 and IP4 are examples of VLIW packets crossing into the subsequent memory line. Looking at figure 8, IP3 is located in memory segments 6-9 in memory lines 0 and 1. It's assumed that IP3 contains two 32-bit compressed instructions for this example. The 32-bit compressed instruction in memory segments 6-7 contains element 117 signaling not-end-of-packet since another compressed 32-bit instruction is in memory segments 8-9. Thus, element 117 will indicate that the subsequent memory line must be read out of the memory to get the

whole VLIW packet to completely decompress the VLIW packet.), the processing unit being arranged to respond to the information by controlling said part of processing as signaled by the information (Miller: Figures 7 and 8, column 11 lines 58-67 continued to column 12 lines 1-25)(IP3 and IP4 have to fetch from the next memory line due to the instruction crossing the memory boundary.), and

wherein the information inserted at compile time signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line (Miller: Figures 3b and 7-8 element 117 and IP3, column 6 lines 31-35 and column 12 lines 4-9)(Element 117 is the information inserted at compile time that tells if an instruction continues into the subsequent memory line. For IP3, this element signals that the A Left address pointer should be updated to fully fetch the IP3 instruction.), so that information following the instruction on the current memory line is skipped over (Miller: Figures 7-8, column 11 lines 35-45)(The pad instruction is the information that is skipped over following the IP3 operation.), the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information (Miller: Figures 7 and 8, column 12 lines 4-9)(For IP3, the A Left address pointer is updated to fully fetch the IP3 instruction in response to element 117.).

10. As per claim 3:

Claim 3 essentially recites the same limitations of claim 1. Therefore, claim 3 is rejected for the same reasons as claim 1.

11. As per claim 6:

Miller disclosed the computer system according to claim 1, the processing unit being a VLIW processing unit containing two or more issue slots for issuing operations from the instruction in parallel to different functional units (Miller: Figures 5, 6, and 9, column 2 lines 27-63), the instructions being VLIW instructions, capable of containing two or more operations (Miller: Figures 5, 6, and 9, column 2 lines 27-63)(The instructions are VLIW instructions that can store two or more instructions.), the instruction comprising a field distinct from the operations to specify said information (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(Element 117 is a separate field that specifies an end-of-block condition.).

12. As per claim 7:

Miller disclosed the computer system according to claim 6, the field comprising, in addition to said information, a decompression code that specifies for which issue slots the instruction contains operations (Miller: Figures 5 and 6, column 5 lines 39-53)(The token indicates the instruction type and "identifies the processing unit.).

13. As per claim 8:

Claim 8 essentially recites the same limitations of claim 1. Claim 8 additionally recites the following limitations:

wherein said controlling comprises at least causing a program counter to skip to a start of a subsequent memory line (Miller: Figures 3b and 7-8 element 117 and IP3, column 6 lines 31-35 and column 12 lines 4-9)(Element 117 is the information inserted at compile time that tells if an instruction continues into the subsequent memory line.

For IP3, this element signals that the A Left address pointer should be updated to fully fetch the IP3 instruction.).

14. As per claims 16:

Miller disclosed the computer system of claim 1 wherein the current memory line and the subsequent memory line are positioned adjacent to the boundary (Miller: Figure 7 element $IP_4$)(The boundary is the crossing between lines 1 and 2. These lines are adjacent to this boundary.).

15. As per claims 17:

Miller disclosed the computer system of claim 1 wherein the fetching of the memory line consists of fetching a single memory line (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(The limitation is interpreted as fetching in view of the 112 second rejection. Miller disclosed that element 117 is inserted at compile time and indicates that the instruction is the last instruction of the memory line. It's obvious to one of ordinary skill in the art that the next instruction is then fetched from memory based on this indication.).

16. As per claims 18:

Claim 18 essentially recites the same limitations of claim 16. Therefore, claim 18 is rejected for the same reasons as claim 16.

17. As per claims 19:

Claim 19 essentially recites the same limitations of claim 17. Therefore, claim 19 is rejected for the same reasons as claim 17.

18. As per claim 20:

Miller disclosed the computer system of claim 1 wherein information inserted at compile time explicitly signals whether or not the subsequent memory line has to be fetched during processing of the instruction, the processing unit being arranged to start fetching of the subsequent memory line in response to the information (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(Miller disclosed that element 117 is inserted at compile time and indicates that the instruction is the last instruction of the memory line. It's obvious to one of ordinary skill in the art that the next instruction is then fetched from memory based on this indication.).

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. 5,819,058), further in view of Keller et al. (U.S. 6,546,478).

20. As per claims 5:

Miller disclosed the computer system according to claim 1.

Miller failed to teach wherein the information signals explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction.

However, Keller disclosed information that signals (Keller: Figure 8 element 126) explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being

arranged to stall in response to the information when the instruction is reached from the branching instruction (Keller: Figure 22 element 192, column 22 lines 1-17, column 23 lines 17-24 and column 26 line 44 continued to column 27 line 8)(The detection of the continuation bit stalls processing until the next page is translated and fetched. The combination adds this bit into the branch instructions of Miller.).

This information, while associated with the instruction and addressed by the same address as the instruction, is stored in a different memory than the instruction. It would also have been obvious to combine the continuation bit 126 in the instruction itself instead of in a separate line predictor entry 82 since it has been held that the use of a one piece construction (instead of the two piece line predictor entry structure and I-cache disclosed in Keller) "would be merely a matter of obvious engineering choice." *In re Larson, 340 F.2d 965,968, 144 USPQ 347,349 (CCPA 1965).*

Adding the continuation bit to the instruction information bits that already exist would allow the processor to know whether a branch target instruction crosses a boundary in the cache and a stall should occur to fetch the next cache line. The processor could detect the need for a memory access quickly and easily if the continuation bit was included in the cache line. The earlier a memory access is known to be needed the better, because it is well known in the art that memory accesses can be costly to processing speed. Specifically in this application, the earlier the memory access is known, the earlier the instruction is fetched from memory and the earlier the instruction can be decompressed and dispatched. It would have been obvious to

combine the continuation bit within the cache line of Miller because of the advantages provided above.

***Response to Arguments***

21. The arguments presented by Applicant in the response, received on 12/8/2009 are partially considered persuasive.

22. Applicant argues "The Office Action asserts that what is claimed isn't prefetching as understood to one of ordinary skill in the art. Instead, the Office Action states that the described act is simply "fetching" data when the data is needed. Applicant has now replaced the term "prefetch" with "fetch" in each of the rejected claims 1, 3, 17 and 19 (and new claim 20 which corresponds to previously canceled claim 2)."

This argument is partially found to be persuasive for the following reason. The examiner has withdrawn the rejection for claims 1, 17, and 19 that recite prefetching. However, the language of prefetching has not been changed in claim 3 and the rejection for claim 3 has been maintained.

23. Applicant argues "In particular, Miller does not disclose "information inserted at compile time that signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line *is skipped over,* ..." (emphasis added). Moreover, not only does Miller lack at least the above recited element, Miller *teaches away from the missing recited element of claimed invention,* in that according to the teaching of Miller the "pad"

instruction that is used to align the next instruction packet *is read out (i. e., considered and identified as a "pad" instruction), and then discarded. See,* Miller, column 12, lines 10-14. Skipping information involves completely disregarding it - i.e., not even reading it. If, as in Miller's system, a pad instruction is "read out" then "the information following the instruction" is not being "skipped over" (as recited in the presently pending claims) - rather, it is being read, identified, and processed as a "pad" instruction" for claims 1 and 8.

This argument is not found to be persuasive for the following reason. The limitation "so that information following the instruction on the current memory line is skipped over" is read on by the "pad instruction." The pad instruction, as shown in figures 7-8, reads as information following the instruction (i.e. IP3) on the current line. The pad instruction is skipped over since it's not executed and is disregarded by the processor for actually processing. Thus, the processor skips over the instruction during execution. The examiner disagrees that skipping information can only involve complete disregard. For example, a student taking a test can read a question and decide to skip the question for the time being and return to answer or not answer the question later. Thus, the definition of skipping something wouldn't include completely disregarding said something.

The examiner notes potential subject matter that could overcome the current rejection. Based on the applicants comments and paragraphs 73 and 84 of the published specification, it appears that multiple fetch bits can be included within instructions to assist with fetching and decoding of the following instructions.

Specifically, it appears that a "realign bit" allows for the next instruction to be realigned at the next memory line. For example looking at figure 8 of Miller, say that IP0 includes such a "realign bit", which would cause fetching of instruction IP1 to start at memory block 8 in element 280 instead of memory block 2. Thus, the data that would be "skipped over" would be memory blocks 2-7. If the examiner is understanding the function of the realign bit with use of the prefetch bit, an amendment containing both of such bits and their functionality would overcome the Miller rejection if correctly claimed.

***Conclusion***

**THIS ACTION IS MADE FINAL.**

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-416262. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, AU 2183